Bipolar Microwave Linear Power Transistor Design

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Abstract—**Design considerations for n-p-n bipolar microwave linear power transistors are discussed. Optimization procedures are presented for determining emitter width for a specific operation frequency, emitter ballasting resistance, and active area geometry based on calculated temperature distributions. A transistor chip designed for 4-GHz operations using these procedures achieved a linear power output of 27.5 dBm at a 1-dB compressed gain of 7 dB with a power added efficiency of 23 percent. Junction temperature rise was limited to 90°C.**

I. Introduction

MICROWAVE bipolar transistor design for power applications involves tradeoffs among effective gain, power, distortion, and reliability. In designing these transistors, decisions on features such as lateral surface geometry, epitaxial-layer specification, and ballasting resistor design usually depend mostly on the experience of the designer and not on analytical techniques. In this paper we will present a more systematic way of designing a bipolar microwave transistor chip for linear class-A operation.

Given a fabrication process which gives suitable gain performance for small-signal low-noise microwave transistors, the first step in linear power transistor design is to determine the emitter width for the best power performance. This is discussed in Section II. The collector operating bias voltage is specified based on the application. Once this is determined, one may choose the epilayer specification by using the guideline given in Section V. The epilayer specification determines the emitter dc density for best linearity. The approximate power-added efficiency can be obtained from experimental data on a small-signal transistor with the same emitter width. Knowing the emitter dc density and the efficiency, the approximate emitter length and base area required for a specific power design can then be estimated. Knowing the base area, one may perform the thermal analysis described in Section III to determine the optimum geometry of the active area. The size of the ballasting resistors is determined by consideration of required gain, metal migration, and temperature limits. The detailed approach for ballasting resistor design is given in Section IV. Finally, the experimental results for a transistor using these procedures are given in Section VI.

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II. Emitter Width Design

A. Distribution of the Microwave Current

It is well known that the high-frequency component of the emitter current is concentrated at the emitter edge. Krishna *et al.* presented an analysis on VHF transistors which includes base conductivity modulation due to injected emitter current [1]. For microwave linear power transistors, however, the attenuation of the microwave signal in the active base region under the base–emitter junction is so large that, in order to obtain good performance, the emitter width has to be so narrow that the dc component of the emitter current density is practically unchanged across the width of the emitter. Also, since the base depth is narrower and base doping density is higher than for lower frequency transistors, the space charge limitation effect occurs at the collector before the carriers injected by the emitter can modify the conductivity in the base. Thus the transistor current is space charge limited, and the average base resistivity stays constant at different RF levels.

Consider the active base region between the emitter and the collector acting as a transmission line with the emitter acting as the ground. The microwave signal travels in both directions transverse to the emitter finger as shown in Fig. 1. Under the linear operating condition, the expression for the microwave voltage across the emitter–base junction at x can be expressed as

$$v_{be}(x) = A_1 \exp(-\gamma x) + A_2 \exp[\gamma(x - x_0)] \quad (1)$$

where x_0 is the emitter width, A_1 and A_2, which will be taken as equal, are the magnitude of the microwave voltage at either side of the emitter, and γ is the wave propagation constant which can be expressed as

$$\gamma = [\rho_b(g_{be} + i\omega c_{eb})]^{1/2} \quad (2)$$

where g_{be} and c_{eb} are the unit area shunt conductance and shunt capacitance of the transmission line, respectively, ω is the angular frequency of the signal, and ρ_b is the active base sheet resistance. Thus

$$g_{be} = qJ_e(1-\alpha)/kT \quad (3)$$

and

$$c_{eb} = C_T + C_D \quad (4)$$

where C_T is the unit area transition capacitance, C_D is the unit area diffusion capacitance, α is the ratio of emitter injection current to the total emitter current, and J_e is the

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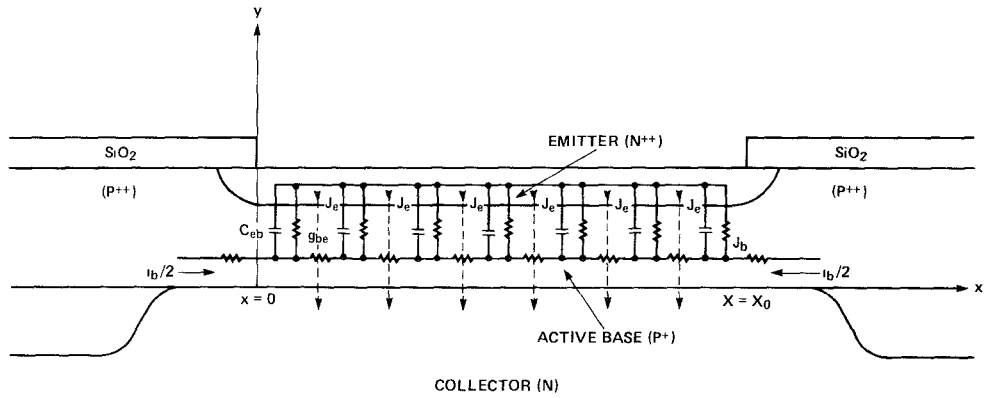


Fig. 1. Transmission line model of emitter–base junction.

dc emitter current density. In the case of the chip design described in Section VI, under normal operating conditioning:

$$I_c = 100 \text{ mA} \qquad T_j \approx 90°\text{C}$$
$$1-\alpha \simeq 1/\beta = 0.02 \qquad \rho_b \approx 10 \text{ k}\Omega/\square.$$

The emitter area A_e is 1.54×10^{-5} cm^2, and the emitter–base transition capacitance and diffusion capacitance at the corresponding collector current are 8.7 and 25 pF, respectively.

Thus at 4 GHz we have

$$\gamma = (1.77+1.65i)\times10^4 \text{ cm}^{-1}. \tag{5}$$

According to (1) and (5), we can see that, in the above mentioned situation, the signal magnitude attenuates to e^{-1} of its original value and the phase shifts 1 rad when it travels about 0.6 μm transverse to the emitter length. Therefore, with $\rho_b = 10$ k$\Omega/\square$, the emitter width should not be too much more than 1.2 μm.

B. Utilization of the Emitter Width

Since having a small base-to-collector capacitance is important for achieving high transistor gain [2], the gain performance of a microwave power transistor improves with increasing microwave current handling capability per unit base area. For the same emitter periphery-to-base area ratio, the best emitter width is not necessarily the smallest. Wider emitters can sometimes give more microwave current capability per unit base area and thus better power performance. An approach for determining the optimum emitter width is given below.

Assuming negligible emitter–base space-charge layer transition time, the emitter microwave current density can be expressed as

$$J_e(x) = g_m v_{be}(x) \tag{6}$$

where

$$g_m = qI_{e0}/(kTA_e) \tag{7}$$

and I_{e0} is the emitter dc. Substituting (1) and (2) into (6) and letting $A_1 = A_2$, we obtain the emitter microwave current density expression

$$j_e(x) = j_{e1}(x) + ij_{e2}(x) \tag{8}$$

where

$$j_{e1}(x) = g_m A_1 \{\exp(-U_1 x)\cos(U_2 x) + \exp[U_1(x-x_0)]\cos[U_2(x-x_0)]\} \tag{9}$$

$$j_{e2}(x) = g_m A_1 \{\exp(-U_1 x)\sin(U_2 x) + \exp[U_1(x-x_0)]\sin[U_2(x-x_0)]\} \tag{10}$$

where U_1 and U_2 are the real and imaginary parts of γ. Thus the magnitude of the microwave component of the emitter current per unit emitter length can be expressed as

$$|i_{em}| = \left\{\left[\int_0^{x_0} j_{e1}(x)\,dx\right]^2 + \left[\int_0^{x_0} j_{e2}(x)\,dx\right]^2\right\}^{1/2}. \tag{11}$$

According to (8)–(10), we see that

$$j_e(0) = j_e(x_0). \tag{12}$$

Letting $j_e(0)$ be constant and assuming uniform dc density across the emitter, a set of $|i_{em}|/|j_e(0)|$[1] versus x_0 curves with the frequency as the parameter is plotted in Fig. 2. One may use this set of curves as a guide for designing the optimum emitter width for a specific frequency.

The curves clearly show that $|i_{em}|/|j_e(0)|$ increases with the emitter width up to a maximum which depends on the frequency of operation. For example, at 4 GHz we can see that the curve starts to turn at $x_0 \simeq 1$ μm and peaks at $x_0 \simeq 1.5$ μm. This indicates that, under the conditions provided for this example, we would want an emitter width of less than 1.5 μm for good power efficiency and more than 1 μm for good output power per emitter length. For a fixed base area, reducing the emitter width will not allow an increased emitter length or a significant increase in the number of emitters. Therefore, a too narrow emitter will result in lower power.

Although this analysis is based on the small-signal condition, it should apply up to the 1-dB gain compression point, since transistor operation will still be approximately linear. Even at higher powers, the curves shown in Fig. 2 can still be used since only first-order accuracy is required.

[1]This quantity is the microwave component of emitter current normalized in the unit of microwave current density at the emitter edge. The quantity is defined as the utilized emitter width.

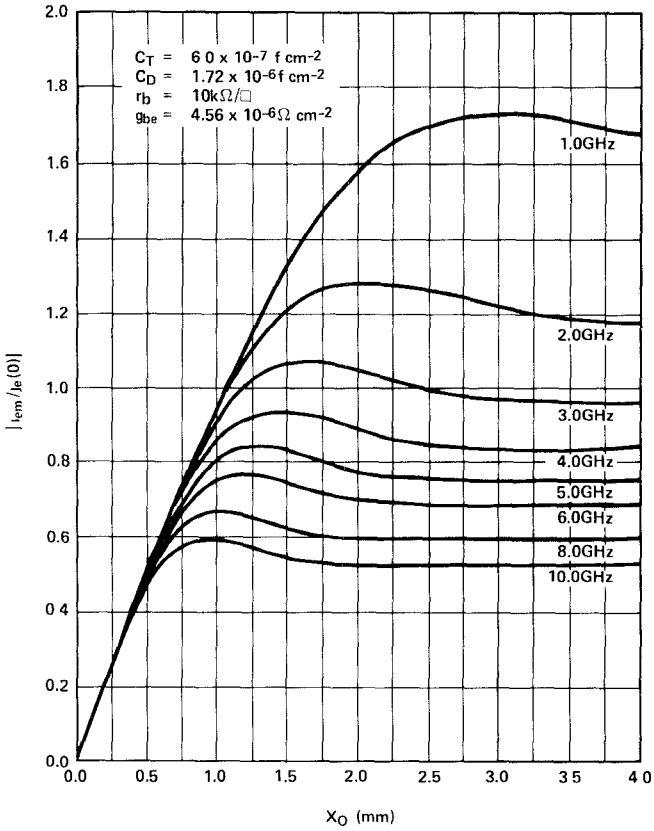


Fig. 2. Dependence of utilized emitter width on emitter width at different frequencies.

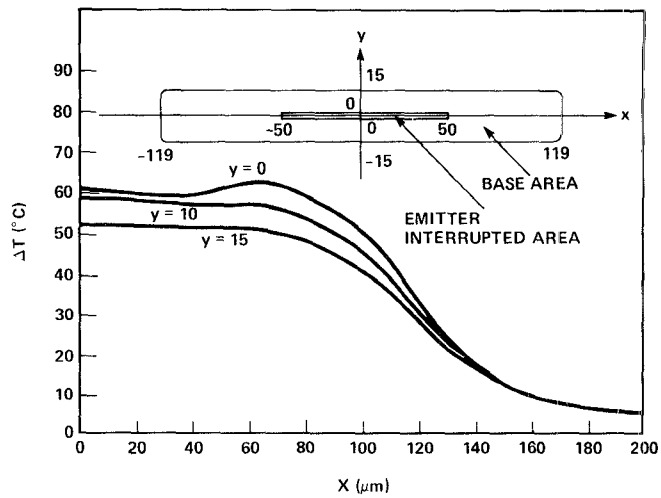


Fig. 3. Calculated temperature distribution curve for a transistor chip (HXTR 5002).

III. Thermal Design

To discuss the thermal design approach, we start with an analysis of the effect of the temperature distribution on the current distribution in the active area. It is well known that emitter current is very sensitive to temperature. However, this applies only to the dc or low-frequency situation. Once the applied microwave signal is large enough that it can affect the dc distribution, the emitter dc is much more evenly spread and insensitive to the temperature distribution [3], [4]. Since a linear power transistor is usually operated in the class-A mode, its dc distribution is very sensitive to the temperature distribution, at least under the small-signal operating conditions. If the transistor is not properly ballasted, dc distribution will be nonuniform, and the transistor cannot operate at a uniform current density for maximum linearity [3]. Thus the linearity under the small-signal condition is degraded. As the microwave signal is increased, the dc becomes more evenly distributed, and the output impedance is changed. Hence, forcing a uniform dc distribution not only enhances linearity but also keeps the impedance more stable and reduces the phase noise. To force a uniform dc distribution, one must keep the temperature as uniform as possible and use ballasting resistors to stabilize the current.

Usually, the active area geometry is designed to minimize temperature variations. The ring geometry is impractical for microwave transistors because of alignment and bonding difficulties. A divided or bar-shaped base area is often used to avoid a large temperature difference between the center and the edges of the active area. Interrupted emitters (see Fig. 6(a)) at the center part of the bar-shaped base will eliminate power dissipation where the transistor would normally be hottest and result in even more temperature uniformity. We used a thermal analysis program [5] to plot the temperature distribution for different base area designs to determine the optimum geometry for the desired linear power. The program was developed based on a paper by Joy and Schlig [6]. Fig. 3 illustrates the calculated temperature-distribution plots using this procedure for the geometry shown in Fig. 6. To decide on such an optimum geometry, many temperature distributions were first plotted and compared for various geometries. Choice of the final geometry was then straightforward.

IV. Ballasting Resistor Design

After choosing a geometry, a high resolution temperature distribution should be plotted assuming uniform dc density for all emitters. To keep the current uniform, the emitters located at the lower temperature regions such as the base area sides can be compensated by using lower values of ballasting resistors to offset a higher emitter–base forward biasing turn-on voltage. However, ballasting resistors cause some phase shift in the emitter current. Therefore, to assure a uniform phase for all the emitter current, one should avoid too much ballasting resistor compensation.

Excessive ballasting can reduce gain, yet not enough ballasting results in nonlinearity and current hogging. The charts shown in Fig. 4(a) and (b) are useful in designing the appropriate amount of ballasting. They show the amount of thermal runaway with fixed collector and base voltages for different ballasting resistors. Thermal resistance (Θ_{jc}) and the collector base voltage are used as the parameters for Fig. 4(a) and (b), respectively. The best choice of the ballasting resistor for an emitter whose Θ_{jc} is

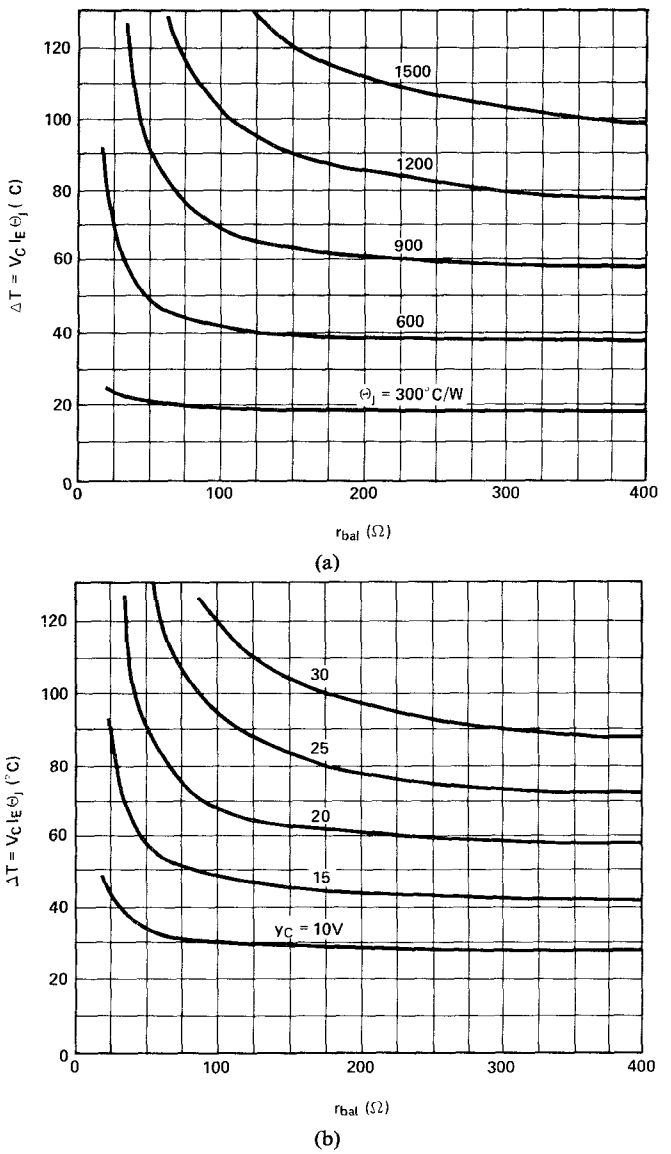


Fig. 4. Curves showing temperature rise after applying a step voltage between base and emitter to obtain a fixed initial collector current (3 mA). The applied collector voltage is fixed at 20 V; Θ_j is the parameter in (a). Θ_j is fixed at 900°C/W, and the applied collector voltage is the parameter in (b).

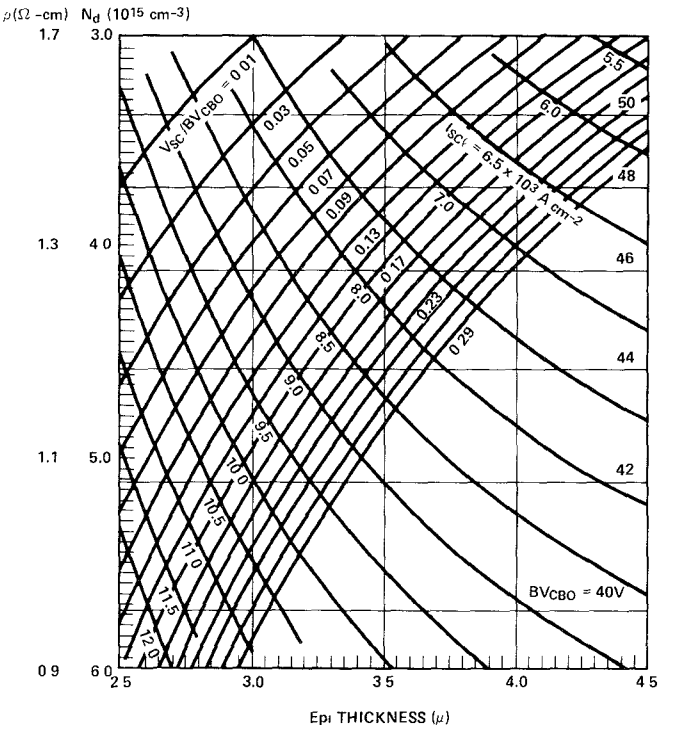


Fig. 5. Epichart. The parameters used are $r_j = 0.5 \times 10^{-4}$ cm, $E_g = 1.2$ eV, $v_d \cong v_{sl} = 7.5 \times 10^6$ cm·s^{-1}, $V_C = 20$ V.

known should be around the knee point of the appropriate curve. Around the knee, a slight change of Θ_{jc}, V_{ce}, or r_{bal} would not create a relatively large amount of ΔT, and r_{bal} would still not be large enough to significantly reduce power and gain. In the case of the transistor whose temperature distribution is shown in Fig. 3, the thermal resistance for an uninterrupted emitter close to the center zone is about 900°C/W. Using the curves in Fig. 5, we find that the appropriate ballasting for such a finger is about 100 Ω. The theory behind the plots in Fig. 4(a) and (b) is as follows.

Consider a bipolar transistor with many emitter fingers. When current hogging occurs, usually some individual fingers draw excessive current and others lose current while the collector voltage and base voltages at each finger remain practically unchanged. Therefore, in looking for an appropriate emitter ballasting resistance, one may consider a transistor with a single emitter of known thermal resistance. With the emitter terminal grounded, the rated voltage to the collector is applied followed by a step voltage to the base terminal so that the transistor will draw a fixed initial current (junction not warmed up yet). As the junction temperature goes up, the emitter current will increase above the initial value to a higher amount depending on both the ballasting resistance and the thermal resistance. The appropriate amount of ballasting resistance should be the amount that does not let the emitter current increase by more than 10–50 percent depending on the design goals.

To calculate this current increase with respect to the ballasting resistance, one may start with the emitter current expression:

$$I_{e0} \cong A_e \frac{qD_{nb}n_i^2}{W_b N_{ab}} \exp\left(qV_j/kT\right) \tag{13}$$

where A_e is the emitter area, D_{nb} is the electron diffusion constant, W_b is the base width, N_{ab} is the base doping density, V_j is the applied voltage across the emitter–base junction, and n_i is the intrinsic carrier density which is expressed as

$$n_i^2 = 1.5 \times 10^{33}\, T^3 \exp\left(-1.2/kT\right). \tag{14}$$

We also have

$$V_j = V_{be} - I_{e0} r_{\text{bal}} - \frac{I_{e0}}{\beta} r_{bb} \tag{15}$$

and

$$T = T_0 + I_{e0} V_c \Theta_j \tag{16}$$

where V_{be} is the voltage applied between the emitter and

the base terminals, r_{bal} is the ballasting resistance, β is the emitter-to-base current ratio, r_{bb} is the total base resistance, T_0 is the heat-sink temperature, Θ_j is the thermal resistance of the emitter to the heat sink, I_{e0} is the emitter dc, and V_c is the collector-to-emitter dc voltage.

Using (13)–(16), one may calculate steady-state I_{e0} for the transistor with different ballasting resistance. $I_{e0}V_c\Theta_j$ versus r_{bal} plots with $V_c=20$ V and different Θ_j as parameters are shown in Fig. 4(a). Similar plots with $\Theta_j=900°C/W$ and different V_c as parameters are shown in Fig. 4(b). In plotting both figures we used $A_e=4.5\times10^{-7}$ cm^{-2}, $N_{ab}=2\times10^{18}$ cm^{-3}, $D_{nb}=7.5$ $cm^2\cdot s^{-1}$, $W_b=1.5\times10^{-5}$ cm, and $I_{e0}(300)=3$ mA, where $I_{e0}(300)$ is the initial emitter finger current before the junction temperature rise. One can see from these curves that the steady-state I_e differs very little from $I_{e0}(300)$ whenever r_{bal} is large enough. However, it runs away from $I_{e0}(300)$ sharply whenever r_{bal} is reduced to below a certain amount. Therefore, one should use a ballasting resistance corresponding to the knee zone of the appropriate curve which is not large enough to excessively reduce the transistor gain and not small enough to create the danger of thermal runaway.

V. Epitaxial Layer Design

A. Current Capacity

The performance and the reliability of a microwave power transistor are very much affected by the resistivity and thickness of its epilayer. Müller has shown the effect of space charge limitation of collector current on the linearity of UHF power transistors [3]. This effect is even more pronounced in the case of microwave power transistors since the microwave current is more crowded at the edge of the emitters which makes the effective collector area become even smaller. Consequently, for linearity and power, it is desirable to have the space charge limited current density J_{SCL} as large as possible. J_{SCL} is expressed as [7]

$$J_{SCL}=qv_dn_0=qv_d\left(N_d+\frac{2\epsilon_sV}{qW_c^2}\right) \tag{17}$$

where v_d is the average drift velocity of carriers in the collector depletion layer, W_c is the width of the collector depletion layer, N_d is the donor density in the layer, V is the applied voltage, n_0 is the moving carrier density at the onset of space charge limitation in the depletion layer, and ϵ_s is the semiconductor permittivity.

B. Ruggedness

The relative amount of collector-base avalanche current a transistor can take before burning the junction is a very important measurement of ruggedness of a transistor. Even some large-area transistors can take only around 1 mA at BV_{CBO} or BV_{CES}, while other much smaller units can take more current even at the same BV_{CBO} and BV_{CES}. The difference in current capability results from different spreading of the avalanche current at the breakdown situation. If the epilayer is thick enough that it is not totally depleted at the avalanche breakdown, there will be enough distributed collector series resistance to keep the current from concentrating at a lower breakdown spot. However, to avoid excessive loss due to collector resistance, microwave transistor epilayers are usually designed to be totally depleted under normal operating conditions. In this situation, the mechanism which forces the avalanching current to spread out is that the breakdown voltage increases with the breakdown current due to the space-charge layer resistance.

Assuming uniform breakdown current density, the total applied voltage at the breakdown current I_{Br} is expressed as [8]

$$V_{Ba}=V_B+I_{Br}R_{SC} \tag{18}$$

where V_B is the voltage at which the avalanche breakdown starts and R_{SC} is the space-charge resistance expressed as

$$R_{SC}=\frac{(W_c-X_A)^2}{2A\epsilon_sv_{sl}} \tag{19}$$

where v_{sl} is the carrier scattering limited velocity, A is the area where breakdown occurs, X_A is the avalanche region width which, according to [8, fig. 10] can be expressed with good approximation as

$$X_A=1.256\times10^{10}\,N_d^{-0.885}\text{ cm}. \tag{20}$$

As long as V_{Ba} is increasing with avalanche current, more spots at the junction will eventually be forced to break down and share the current. However, as soon as the avalanche current density at any spot reaches the space-charge neutralizing current density J_0, the avalanche injection second breakdown [9] then occurs at the spot. This results in the spot drawing a large amount of current which will lead to burnout. The space-charge neutralizing current can be expressed as

$$J_0=qv_{sl}N_d. \tag{21}$$

The difference in voltage between the beginning of avalanche breakdown and the stage immediately before the second breakdown should be approximately the same as the space-charge resistive voltage which is expressed as [10]

$$V_{SC}\equiv J_0\rho_{SC}=J_0R_{SC}A \tag{22}$$

where ρ_{SC} is the space-charge resistivity in $\Omega\cdot cm^2$. Apparently, the larger the value of V_{SC}/V_B the more the avalanche current will be forced to spread out to the other areas before any spot reaches avalanche injection second breakdown. Therefore, devices with epilayers that result in higher V_{SC}/V_B will be more rugged.

C. Breakdown Voltage

The avalanche breakdown between the collector and the base for microwave power transistors starts at the cylindrical edge of the base–collector junction. Usually, the epilayer of the microwave power transistor is thick enough and its doping density is high enough that the

breakdown voltage is independent of the epitaxial thickness. (This corresponds to the upper left corner of [11, fig. 5]. The expression for V_B under this circumstance is [8]

$$V_B = 60\left(\frac{E_g}{1.1}\right)^{3/2}\left(\frac{N_d}{10^{16}}\right)^{-3/4}\left\{\left[\left(2+\frac{r_j}{w}\right)\frac{r_j}{w}\right]^{1/2}\frac{r_j}{w}\right\} \quad (23)$$

where E_g is the band gap in electron volts, r_j is the base diffusion depth, W is the theoretical depletion layer width at breakdown voltage which, according to [8, fig. 25], can be expressed as

$$W = 6.41\times 10^{9} N_d^{-0.837} \text{ cm}.$$

An epichart consisting of three families of curves using V_B, J_{SCL}, and V_{SC}/V_B as parameters is shown in Fig. 5 to illustrate the epilayer design approach.

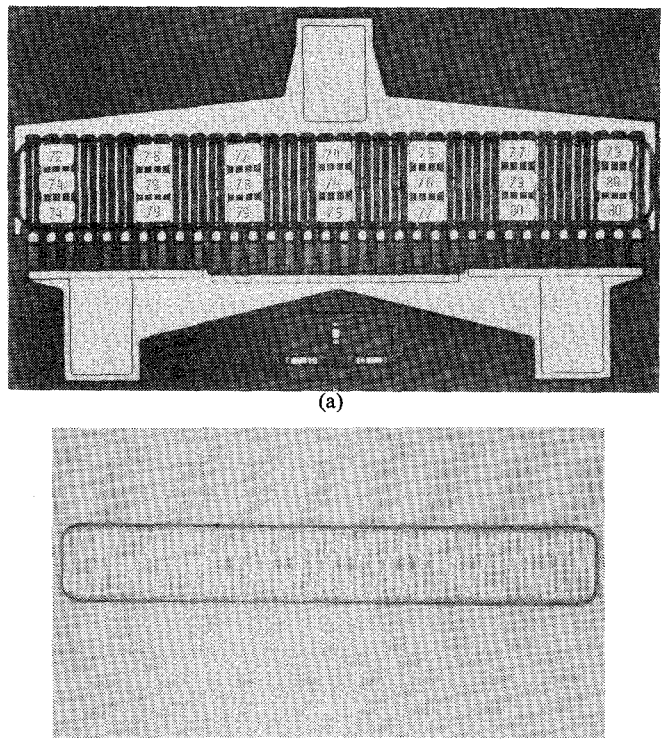
For power and linearity, one would tend to specify the epilayer for higher J_{SCL} [3], [11], which means a design toward the lower left corner of the epichart. For more ruggedness, one would go toward the lower right corner where V_{SC}/V_B is larger. For higher breakdown, one would move the epilayer specification toward the upper part of the epichart. Thus the epilayer specification is a compromise among these three choices and can be in a triangle in the epichart. Each side of the triangle is bounded by one curve from each of the three families.

VI. Design and Experimental Results

An n-p-n linear power transistor intended primarily for the 3.7–4.2-GHz frequency range was designed according to the methods mentioned in the previous sections to achieve a power output at the 1-dB gain compression point of 27 dBm. Tests indicate that the device easily achieves the expected performance.

As was discussed in Section II-B, to operate around 4 GHz, the emitter width should be between 1.0 and 1.5 μm. Since the device was intended to be biased at a collector voltage of 20 V in common emitter form, the collector–base breakdown voltage should be in excess of 40 V. Therefore, according to the epichart, the epilayer resistivity should be more than 1.0 $\Omega\cdot$cm. In order for the device to take a high enough current at BV_{CBO} breakdown, the epilayer should be specified so that the ratio V_{SC}/BV_{CBO} should be larger than 0.1. These, together with the desire for higher space-charge limited current and the necessity of some guard zone in specifying the epilayer, lead us to specify a resistivity of around 1.1 $\Omega\cdot$cm and a thickness of 2.7–2.9 μm. Thus we have, according to the epichart, $J_{SCL} = 11\times 10^{3}$ A$\cdot$cm^{-2}.

Since J_{SCL} is roughly the upper limit of the current density swing during high-frequency operation, the dc emitter current density should be put between 50 and 60 percent of J_{SCL} in order to obtain the best linearity. We chose to bias it at 60 percent of J_{SCL} to achieve more power. This means the dc density is around 6.6×10^{3} A$\cdot$cm^{-2}. The data obtained from small-signal devices indicated that the efficiency is about 20–25 percent. Thus we put the dc bias at $V_{CE} = 20$ V, $I_c = 100$ mA. Consequently, the total emitter length for this device has to be about 1 mm.



(a)

(b)

Fig. 6. (a) Interdigitated emitter and base contact windows of the linear power transistor. Central interrupted emitters result in more uniform temperature distribution. (b) Hewlett–Packard HXTR-5002 transistor chip and its temperature distribution as monitored by an infrared microscope (bias: $V_{ce} = 18$ V, $I_c = 110$ mA).

It was decided that, for this total emitter length, the input impedance per cell would not be too low even if we put all the emitter fingers in one cell. Thermal analysis indicated that the geometry as shown in Fig. 6 (a) and (b) give good temperature uniformity. A single cell design will also eliminate multicell-chip problems such as uneven phase shift and uneven temperature distribution between cells. After deciding the metal finger size and spacing based mainly on the metal migration consideration, the dimension of the base area was finally fixed to be 34×242 μm. In the base area, there are totally 34 emitter fingers with the center 14 fingers being interrupted for 4 μm at the middle for cooling purposes (see Fig. 6(a)).

The size of the thin film Ta_2N ballasting resistors was determined in such a way that it would not have more than a 20°C temperature rise from the substrate directly underneath it. There is some adjustment of the ballasting resistor value for those cooler emitter fingers located at the sides of the base area and for those emitter fingers which are interrupted. Actual measurement in large quantities of this device shows that the performance, ruggedness, and temperature distribution are as expected.

The transistor can tolerate infinite VSWR at least at frequencies higher than 2 GHz. This is due mainly to the specification of the epilayer to have high enough BV_{CBO} and V_{SC}/BV_{CBO}. This also prevents the transistor from

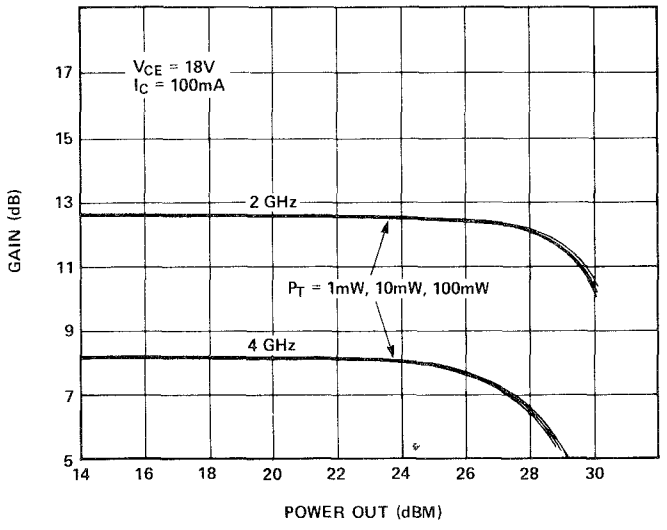


Fig. 7. Gain versus power plots at 2 and 4 GHz. The closeness of the curves tuned for maximum gain at different levels of input power P_T indicates that the transistor impedance is independent of the power level.

being easily destroyed due to mishandling during a test. The temperature distribution predicted, as shown in Fig. 3, was checked by using an infrared microscope. Fig. 6(b) shows the measured temperature distribution of a chip mounted on a thin BeO substrate on a copper bar when biased at the rated dc bias condition of 18 V, 110 mA. We can see that if one adds the 25°C room temperature to ΔT in Fig. 3, the data on Figs. 3 and 6(b) are very close. The uniformity of temperature is the result of employing the narrow bar-shaped base area and interrupted emitters at the center of the base area. This geometry could not have been used with confidence if we did not have the accurate analysis program as mentioned in Section III. As a result of this forced uniform temperature distribution, the output impedance of this device is independent of the signal level. The near equivalence of gain versus power output curves for both small- and large-signal tuning is illustrated in Fig. 7. This makes it easier to design a circuit for this device, because small-signal S parameters can be used for large-signal design. This is usually not true for most microwave power transistors. Fig. 8 illustrated the typical 1-dB compressed power and gain versus frequency and current for this transistor chip in a partially matched stripline package [12].

VII. Conclusion

With a known process which gives good performance at microwave frequencies for small transistors, one may design linear power transistors by deciding emitter width using the chart shown in Fig. 2. The temperature distribution on a chip with a desired linear power capability should be accurately plotted for different geometries to determine the optimum geometry of the active area. Ballasting resistors can be individually designed for each emitter by plotting temperature rise versus ballasting resistance curves. The epilayer specification is critical for achieving the desired power, ruggedness, operation voltage, and linearity. The epichart shown in Fig. 5 can be used to obtain the best compromise. An actual device designed using this approach has been shown to be rugged with good class-A performance at 4 GHz.

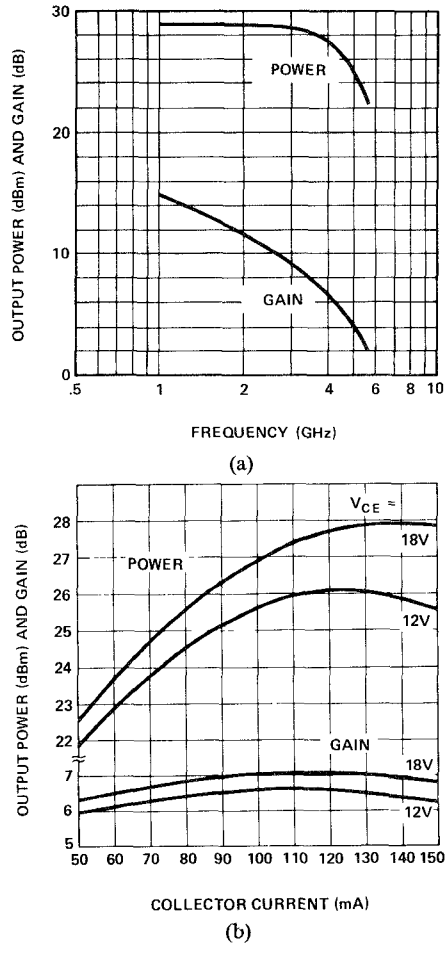


Fig. 8. (a) 1-dB compressed gain and the associated output power versus frequency curves for the transistor chip in a partially input matched stripline package. (b) 1-dB compressed gain and the associated output power versus collector current curves at $V_{ce} = 12$ and 18 V for the transistor chip in a partially input matched stripline package.

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Improvement of a Class-C Transistor Power Amplifier by Second-Harmonic Tuning

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Abstract—**Considerations for the effects of second-harmonic reactive terminations on the performances of a UHF class-C transistor power amplifier are presented. An experimental amplifier circuit design using coupled-TEM-bar transmission lines is described. This circuit can vary the fundamental and the second-harmonic impedance terminations of the amplifier independently. With this amplifier circuit, significant improvement in the performance characteristics of a class-C power amplifier were achieved by presenting proper values of second-harmonic reactive terminations, both at the input and the output of the transistor.**

I. Introduction

In POWER amplifiers, the transistor is operated as a nonlinear device under large-signal conditions. In certain situations (such as for class-C operation), the nonlinearity of the device generates significant amounts of harmonic components [1]. Furthermore, changes in the impedances presented to the transistor at the harmonic frequencies, while maintaining the same fundamental frequency impedances, result not only in changes in the relative values of the harmonic frequency components but also in different values of the fundamental frequency component. Thus for a good design method to accurately predict the performance characteristics of power amplifiers, one must take into account the significant effects of the source and the load terminating impedances at the harmonic frequencies [2], [7].

In the present work it is considered that the second harmonic is the most dominant of all harmonic components. This assumption may be justified by the fact that the transistor package tends to attenuate the third and higher harmonics considerably.

The purpose of this paper is to study the effects of second-harmonic reactive terminations on the performance characteristics of a class-C UHF transistor power amplifier. For this purpose, a coupled-TEM-bar circuit has been designed [3]–[5]. Two such circuits have been used, one at the input and the other at the output port of the transistor. These coupled-TEM-bar circuits can be adjusted to have an important property, i.e., that one can vary the fundamental and the second-harmonic impedances presented to the transistor terminals in a quite independent manner. This characteristic thus allows us to study the effects of varying the second-harmonic terminations on the performances of the amplifier. It is shown in this paper that a significant improvement in the performance characteristics (such as power output, dc-to-RF conversion efficiency and power gain) of a class-C transistor power amplifier can be achieved by proper choice of the second-harmonic reactive terminations of the amplifier.

In the following, the characteristics of the coupled-TEM-bar circuit are described with reference to the actual amplifier circuit. Experimental performances of the amplifier are also presented.

II. Experimental Amplifier Circuit

The experimental amplifier circuit has been designed using two coupled-TEM-bar circuits [3]–[5], one at the

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